REMARKS

Applicant has reviewed and considered the Office Action mailed on September 3, 2003, and the references cited therewith.

Claims 1, 8, 9, 13, 14, 20, and 21 are amended, no claims are canceled, and claims 31-36 are added; as a result, claims 1-36 are now pending in this application. The amendments to the claims are fully supported by the specification as originally filed. No new matter is introduced. The amendments are made to clarify the claims. Applicant respectfully requests reconsideration of the above-identified application in view of the amendments above and the remarks that follow.

Amended claims 1, 8, 9, 13, 14, 20, and 21 find support, for example, in the specification on page 8, lines 24-27.

New claims find support, for example, in reference U.S. 6,320,222, which was co-filed and incorporated by reference in the original application of the instant application, in column 11, lines 10-16, and previously amended into the specification of the instant application.

Double Patenting Rejection

Claims 1-30 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-22 of U.S. Patent No. 6,320,222 taken with Mazure (U.S. 5,308,782).

A Terminal Disclaimer will be considered when all claims are indicated to be otherwise allowable.

§112 Rejection of the Claims

Claims 1-13 and 21-31 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed had possession of the claimed invention; and/or as based on a disclosure which is not enabling. Applicant respectfully traverses these grounds for rejection of these claims.

Independent claims 1, 8, 9, 13, and 21 are amended to expedite the processing of the instant application. Applicant submits that the amended independent claims and the claims that depend on these independent claims are in condition for allowance.

Applicant requests withdrawal of these rejections of claims 1-13 and 21-31, and reconsideration and allowance of these claims.

§102 Rejection of the Claims

Claims 14-19 were rejected under 35 USC § 102(e) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Bertin et al. (U.S. 6,060,746). Applicant traverses these grounds for rejection.

Applicant reserves the right to swear behind Bertin et al. (hereafter Bertin) at a later date. Nevertheless, Applicant respectfully submits that the claims are distinguishable over Bertin for the reasons stated below.

Bertin deals with a power transistor, which is defined by Bertin in column 1, lines 55-60, "as a plurality of individual transistors of the same conductivity type that are formed on a common substrate, where the source electrodes each share a common conductive connection layer and the drain electrodes of the transistors also each share a common conductive connection layer." Further Bertin's power transistor has a single gate control. *See Bertin Summary column 2, 38-42, Summary column 1, 60-63, and column 4, lines 7-10.* Applicant can not find in Bertin a teaching or suggestion of forming a first gate with a contact to couple to a first voltage source and forming a second gate with a contact to couple to a second voltage source, as recited in claim 14. Thus, Applicant submits that Bertin does not anticipate claim 14, and claim 14 is patentable under 35 USC 102 over Bertin.

In addition to Bertin providing no teaching or suggestion of a first gate with a contact to couple to a first voltage source and a second gate with a contact to couple to a second voltage source, there is no motivation to form such gates. Forming first and second gates as recited in claim 14, would be contrary to Bertin, since Bertin teaches forming a single power transistor with a single control gate structure, as demonstrated by the abovementioned cited sections dealing with Bertin's power transistor. Thus, Bertin does not establish a proper *prima facie* case

of obviousness with respect to claim 14, and claim 14 is patentable under 35 USC 103 over Bertin.

Claims 15-19 depend on claim 14 and are patentable over Bertin for the reasons stated above and additionally in view of the further elements of these dependent claims.

Applicant requests withdrawal of these rejections of claims 14-19, reconsideration and allowance of these claims.

First §103 Rejection of the Claims

Claims 1-26 were rejected under 35 USC § 103(a) as being unpatentable over Mazure et al. (U.S. 5,308,782) taken with Colinge (Article of "Reduction of Kink Effect...."). Applicant traverses these grounds for rejection.

Mazure et al. (hereafter Mazure) deals with vertically stacking transistors in a memory device. With respect to Mazure, the Office Action states:

> "Mazure lacks to form the body region as a fully depleted structure. However, Colinge teaches to form a thin film transistor comprising a thin body channel region as fully depleted structure (page 97, left column; page 99), wherein the body region having a thickness of about 100nm."

Colinge deals with a horizontal transistor structure having a gate on a gate oxide and a backside gate, not on a gate oxide, but on the back on the substrate on which the horizontal transistor is formed. There is no teaching or suggestion in Colinge regarding a vertical transistor structure having a body region as a fully depleted structure. The Office Action has not provided a reference to support the modification of Colinge and Mazure as proposed in the Office Action.

The Office Action states:

> "it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor body region of Mazure to have a thin thickness as taught by Colinge as to form the thin film transistor comprising s thin body channel region as fully depleted structure. This is because of the desirability to reduce kink effect, current overshoots, and to form a very thin transistor."

As noted in the opening sentences of the first paragraph of Colinge, these desirable effects noted in the above quote, are related to problems whose origins arise from a horizontal silicon-on-insulator n-channel MOSFET and are floating-substrate effects. Mazure addresses the problems

of planar transistors with vertical transistor structures, where the initial vertical transistor in the structure is fabricated up from the substrate starting with a diffusion region (14) on which a drain region (28) is formed. It appears that Mazure does not need to the address floating-substrate effects identified in Colinge. Thus there is no motivation to combine Colinge with Mazure. The fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP § 2143.01. Applicant submits that the Office Action has not provided a reference suggesting the desirability of the combination and modification of the cited references, given that Mazure deals with vertical transistor structures and Colinge deals with a horizontal transistor structure, and the reasons for the combination provided in the Office Action do not appear to apply.

In addition, Applicant can not find a teaching or suggest in Mazure for a first gate on a first oxide layer where the first gate has a contact to couple to a first voltage source, and a second gate on a second oxide layer, where the second gate has a contact to couple to a second voltage source, as recited in claim 1. Mazure has an embodiment that allows a double gated transistor *(See Mazure, column 7, lines 48-61)*, but Applicant can not find a teaching or suggestion that the Mazure double gates are configured to couple to two voltage sources as recited in claim 1. On the contrary, Mazure indicates that the double gates (18 and 19) are formed collectively as a single gate (*See Mazure, column 7, lines 59-61)*. Further, in column 10, lines 52-68, Mazure notes that the structures shown in Figs. 1-21 can be used in a vertical transistor stack in the circuit of Figure 22, which does not teach or suggest a double gated transistor in which each gate has a contact to couple to different voltage sources.

Colinge does not cure the abovementioned deficiencies of Mazure. Therefore, for at least the above reasons, Applicant respectfully submits that the combination of Mazure and Colinge does not teach or suggest all the elements as recited in claim 1. Thus, the combination of Mazure and Colinge does not establish a proper prima facie case of obviousness with respect to claim 1, and claim 1 is patentable over Mazure in view of Colinge.

As amended, independent claims 8, 9, 13, 14, 20, and 21 recite similar elements as claim 1 and are patentable over Mazure in view of Colinge for the reasons stated above and additionally in view of the further elements of these independent claims.

Claims 2-7, 10-12, 15-19, and 22-26 are dependent on claims 1, 9, 14, and 21, respectively, and are patentable over Mazure in view of Colinge for the reasons stated and additionally in view of the further elements of these dependent claims.

Applicant respectively requests withdrawal of these rejections of claims 1-26, and reconsideration and allowance of these claims.

Second §103 Rejection of the Claims

Claims 1-30 were rejected under 35 USC § 103(a) as being unpatentable over Bertin et al. (U.S. 6,060,746) taken with Mazure et al. (U.S. 5,308,782). Applicant traverses these grounds for rejection.

Bertin deals with a power transistor, which is defined by Bertin in column 1, lines 55-60, "as a plurality of individual transistors of the same conductivity type that are formed on a common substrate, where the source electrodes each share a common conductive connection layer and the drain electrodes of the transistors also each share a common conductive connection layer." Further Bertin's power transistor has a single gate control. *See Bertin Summary column 2, 38-42, Summary column 1, 60-63, and column 4, lines 7-10.* Applicant can not find in Bertin a teaching or suggestion of forming a first gate with a contact to couple to a first voltage source and a second gate with a contact to couple to a second voltage source, as recited in claim 1.

In addition to Bertin providing no teaching or suggestion of a first gate with a contact to couple to a first voltage source and a second gate with a contact to couple to a second voltage source, there is no motivation to form such gates. Forming first and second gates as recited in claim 1, would be contrary to Bertin, since Bertin teaches forming a single power transistor with a single control gate structure, as demonstrated by the abovementioned cited sections dealing with Bertin's power transistor.

As discussed above, Mazure also does not teach or suggest forming a first gate with a contact to couple to a first voltage source and a second gate with a contact to couple to a second voltage source, as recited in claim 1. Mazure does not cure the deficiencies of Bertin. Therefore, Applicant submits that the combination of Bertin and Mazure does not teach or suggest all the elements of claim 1. Thus, the combination of and Mazure does not establish a

proper *prima facie* case of obviousness with respect to claim 1, and claim 1 is patentable over Bertin in view of Mazure.

As amended, independent claims 8, 9, 13, 14, 20, and 21 recite similar elements as claim 1 and are patentable over Bertin in view of Mazure for the reasons stated above and additionally in view of the further elements of these independent claims.

Claims 2-7, 10-12, 15-19, and 22-30 are dependent on claims 1, 9, 14, and 21, respectively, and are patentable over Bertin in view of Mazure for the reasons stated and additionally in view of the further elements of these dependent claims.

Applicant respectively requests withdrawal of these rejections of claims 1-30, and reconsideration and allowance of these claims.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 371-2157) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 3rd day of December, 2003.

Amy Moriarty
Name

Signature